Design of a FET (Transistor)

\[
N_A = \frac{6.023 \times 10^{23}}{\text{mole}} \quad e = 1.6 \times 10^{-19} \text{ Coul}
\]

\[
k_B = \frac{1.38 \times 10^{-23}}{\text{Joule/K}} \quad h = 6.63 \times 10^{-34} \text{ J} \cdot \text{s}
\]

\[
? m = 10^{-6} \text{ m} \quad \text{pF} = 10^{-9} \text{ F}
\]

\[
?_o = 8.85 \times 10^{-12} \frac{\text{F}}{\text{m}}
\]

---

![Design of a FET (Transistor)](image)

**Figure 8.27** Schematics of a MOSFET with the p-type base n-doped for source and drain. A contact is attached directly to the substrate for threshold voltage adjustment. (After K.W. Böer, Survey of Semiconductor Physics, Vol. 2, Van Nostrand Reinhold, New York, 1992. With permission.)

\[
I_D = \left( \frac{Z}{L} \right) \mu_c C_0 \left[ V_S - 2V_T - \frac{E_D}{2} \right] V_{DS} - \frac{2}{3C_0} \left( 2eE_D N_A \right)^{\frac{1}{3}} \left[ \left( V_{DS} + 2V_T \right)^{\frac{1}{3}} - \left( 2V_T \right)^{\frac{1}{3}} \right]
\]  

(8.37)

where \( C_0 \) is the gate SiO₂ layer's capacitance per unit area and

\[
V_T = \frac{k_B T}{e} \ln \left( \frac{N_A}{n_i} \right)
\]

For \( Z \) and \( L \), see Figure 8.27.