Design of a FET (Transistor)

N_A ?? $6.023?10^{23}?\frac{1}{mole}$

k_B ?? $1.38?10^{?\,23}?\frac{joule}{K}$

e ?? $1.6?10^{?\,19}?coul$

h ?? $6.63?10^{?\,34}?J?s$

?m ?? $10^{?\,6}?m$

$?_o$?? $8.85?10^{?\,12}?\frac{F}{m}$

pF ?? $10^{?\,9}?F$

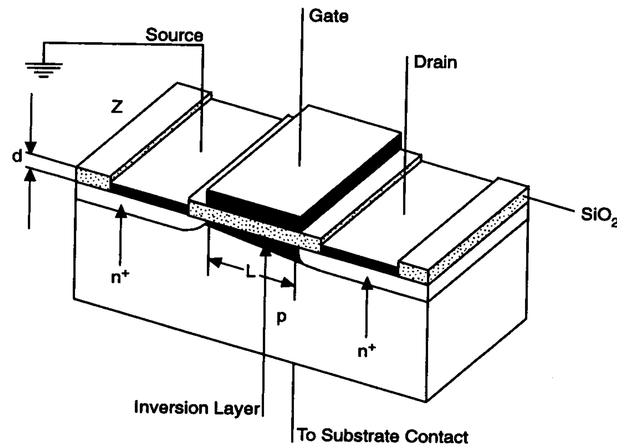

Figure 8.27 Schematics of a MOSFET with the p-type base n+-doped for source and drain. A contact is attached directly to the substrate for threshold voltage adjustment. (After K.W. Böer, *Survey of Semiconductor Physics*, Vol. 2, Van Nostrand Reinhold, New York, 1992. With permission.)

$$I_D = \left(\frac{Z}{L}\right)\mu_n C_0 \left\{ \left(V_g - 2V_T - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2}{3C_0}\left(2\varepsilon\varepsilon_0 e N_A\right)^{1/2}\left[\left(V_{DS} + 2V_T\right)^{3/2} - \left(2V_T\right)^{3/2}\right] \right\} \quad (8.37)$$

where C_0 is the gate SiO_2 layer's capacitance per unit area and

$$V_T = \frac{k_B T}{e} \ln\left(\frac{N_A}{n_i}\right).$$

For Z and L, see Figure 8.27.